STL7N6LF3

Automotive-grade N-channel 60 V, 35 mΩ typ., 6.5 A STripFET™ F3 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

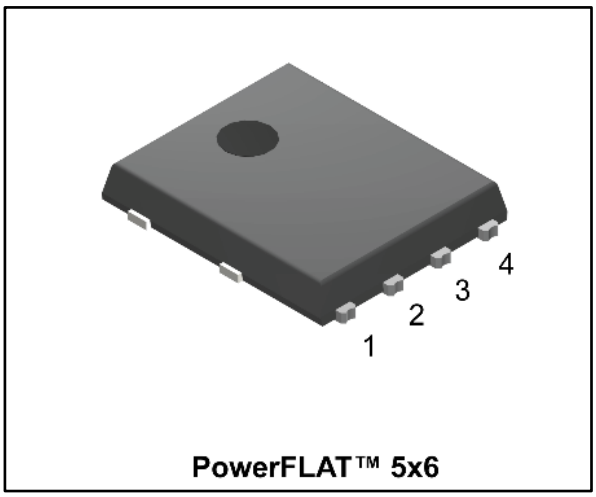
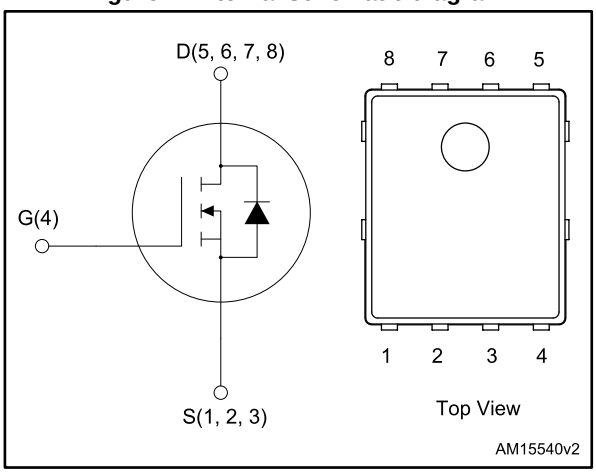


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL7N6LF3	60 V	43 mΩ	6.5 A

- AEC-Q101 qualified
- Logic level $V_{GS(th)}$
- 175 °C maximum junction temperature
- 100% avalanche rated
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1: Device summary

Order code	Marking	Package	Packing
STL7N6LF3	7N6LF3	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	20	A
I_D (1)	Drain current (continuous) at T_c = 100 °C	16	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	6.5	A
I_D (2)	Drain current (continuous) at T_{pcb} = 100 °C	4.6	A
I_{DM} (3),(2)	Drain current (pulsed)	26	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	52	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25°C	4.3	W
I_{AV}	Not-repetitive avalanche current	6.5	A
E_{AS} (4)	Single pulse avalanche energy	190	mJ
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

Notes:

(1) This value is rated according to $R_{thj\text{-}case}$

(2) This value is rated according to $R_{thj\text{-}pcb}$

(3) Pulse width limited by safe operating area.

(4) Starting T_J= 25 °C, I_D= 8 A, V_{DD}= 25 V.

Table 3: Thermal resitance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.9	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	35	°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3 A		35	43	mΩ
		V_{GS} = 5 V, I_D = 3 A		48	60	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	432	-	pF
C_{oss}	Output capacitance		-	93	-	
C_{rss}	Reverse transfer capacitance		-	10.5	-	
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 6.5 A, V_{GS} = 0 to 10 V (see *Figure 13: "Test circuit for gate charge behavior"*)	-	8.7	-	nC
Q_{gs}	Gate-source charge		-	1.9	-	
Q_{gd}	Gate-drain charge		-	1.9	-	
R_G	Intrinsic gate resistance	f =1 MHz, ID=0 A	-	6.3	-	Ω

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 3 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 12: "Test circuit for resistive load switching times"* and *Figure 17: "Switching time waveform"*)	-	6.7	-	ns
t_r	Rise time		-	10.4	-	
$t_{d(off)}$	Turn-off delay time		-	32.4	-	
t_f	Fall time		-	5.4	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		26	A
V_{SD}(2)	Forward on voltage	I_{DS} = 6.5 A, V_{GS} = 0 V	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 6.5 A, di/dt = 100 A/µs V_{DD} = 48 V, T_j = 150 °C (see *Figure 14: "Test circuit for inductive load switching and diode recovery times"*)	-	24		ns
Q_{rr}	Reverse recovery charge		-	23.3		nC
I_{RRM}	Reverse recovery current		-	1.9		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

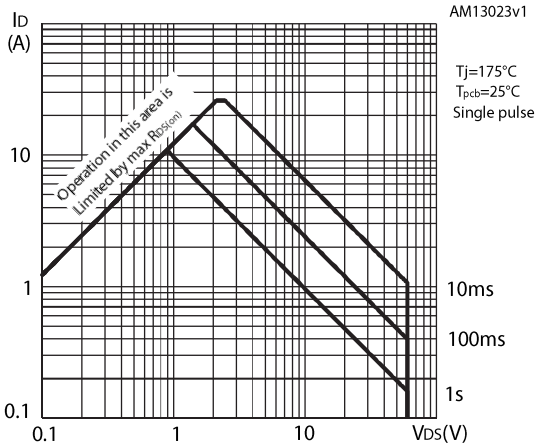


Figure 3: Thermal impedance

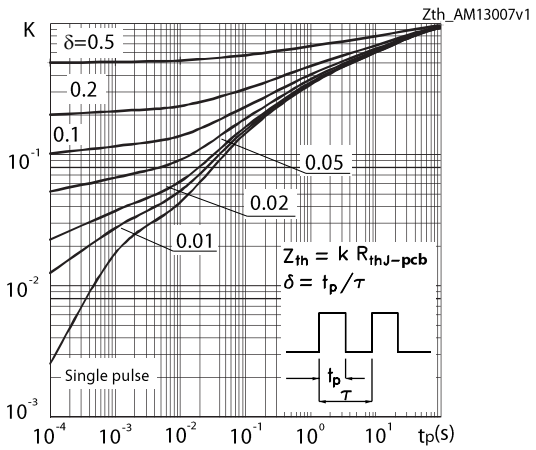


Figure 4: Output characteristics

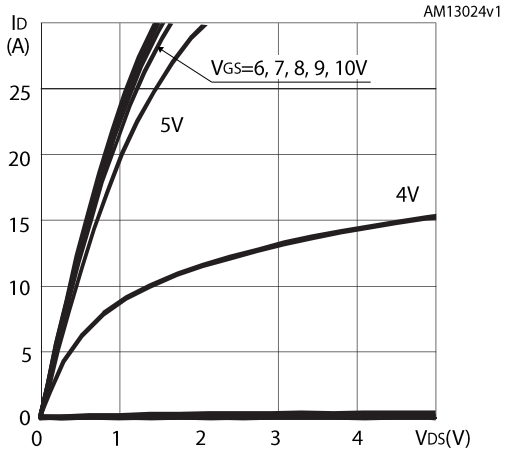


Figure 5: Transfer characteristics

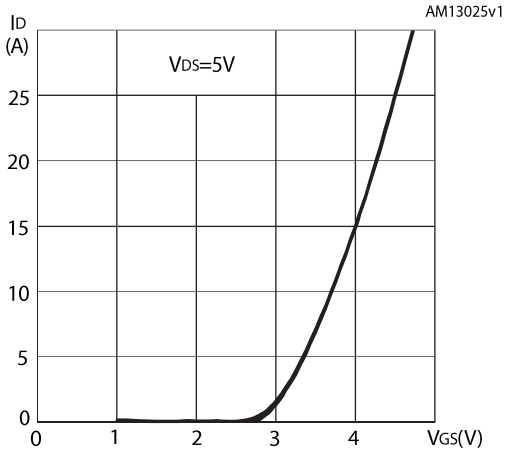


Figure 6: Normalized $V_{(BR)DSS}$ vs temperature

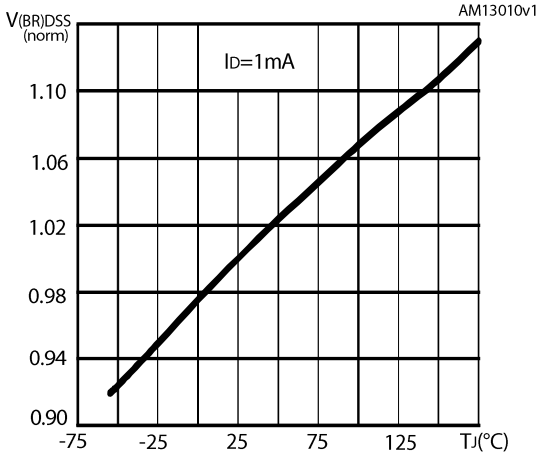


Figure 7: Static drain-source on-resistance

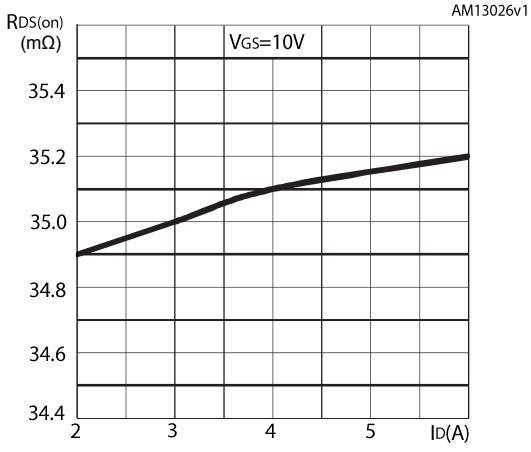


Figure 8: Gate charge vs gate-source voltage

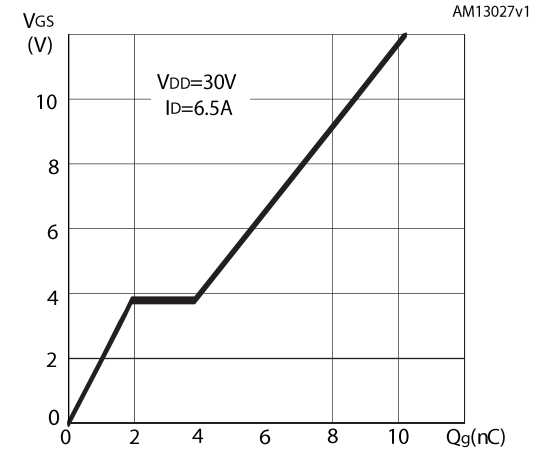


Figure 9: Capacitance variation

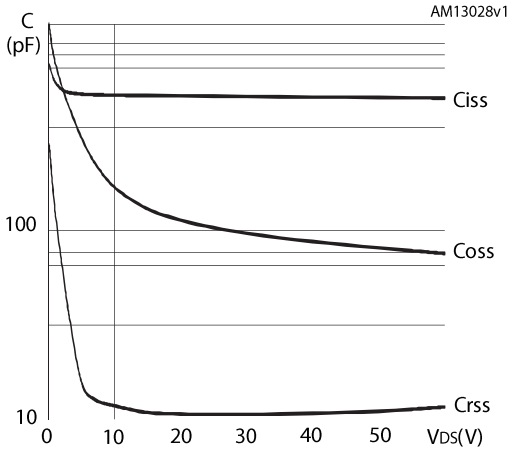


Figure 10: Normalized gate threshold voltage vs temperature

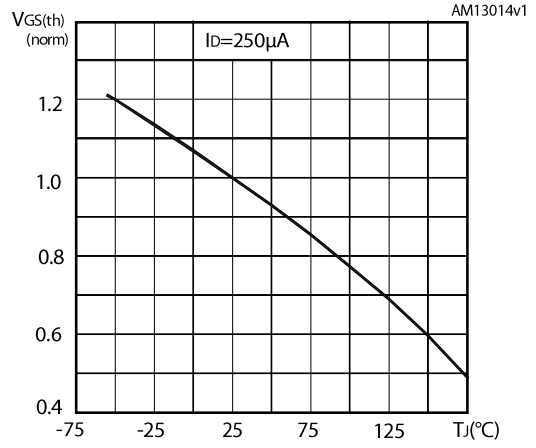
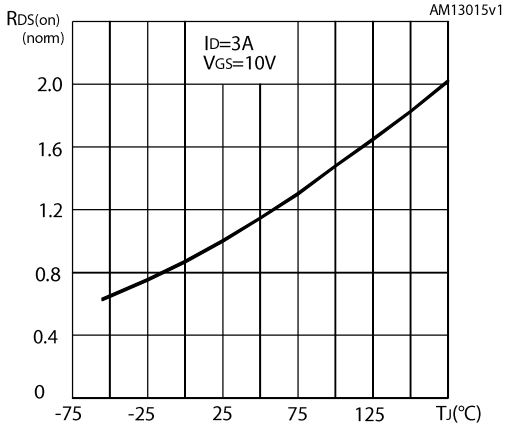


Figure 11: Normalized on-resistance vs temperature



3 Test circuits

Figure 12: Test circuit for resistive load switching times

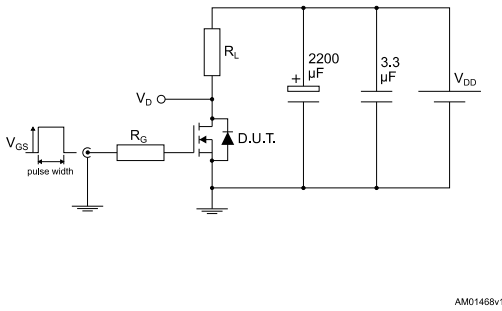


Figure 13: Test circuit for gate charge behavior

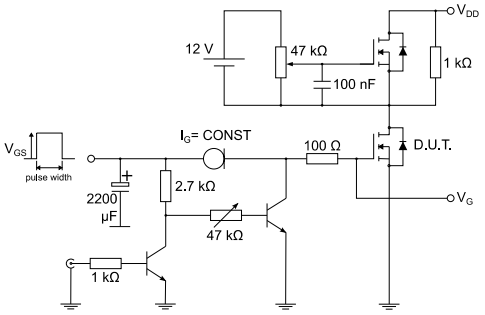


Figure 14: Test circuit for inductive load switching and diode recovery times

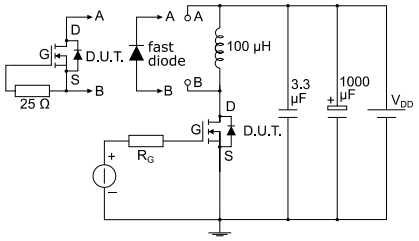


Figure 15: Unclamped inductive load test circuit

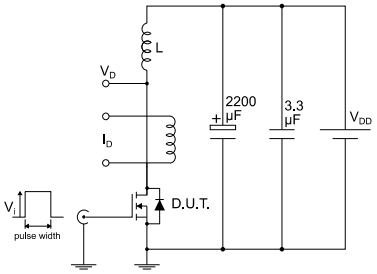


Figure 16: Unclamped inductive waveform

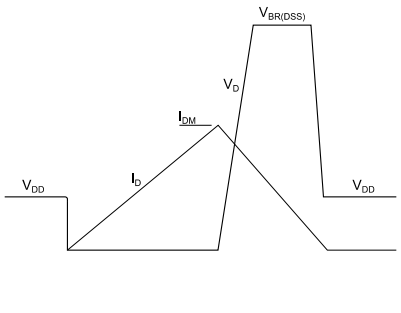
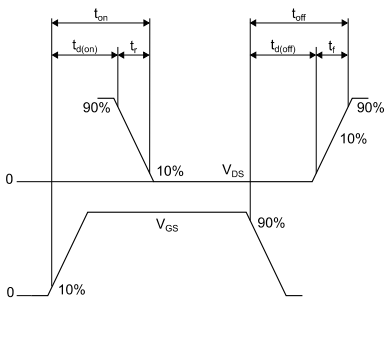


Figure 17: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 WF type R package information

Figure 18: PowerFLAT™ 5x6 WF type R package outline

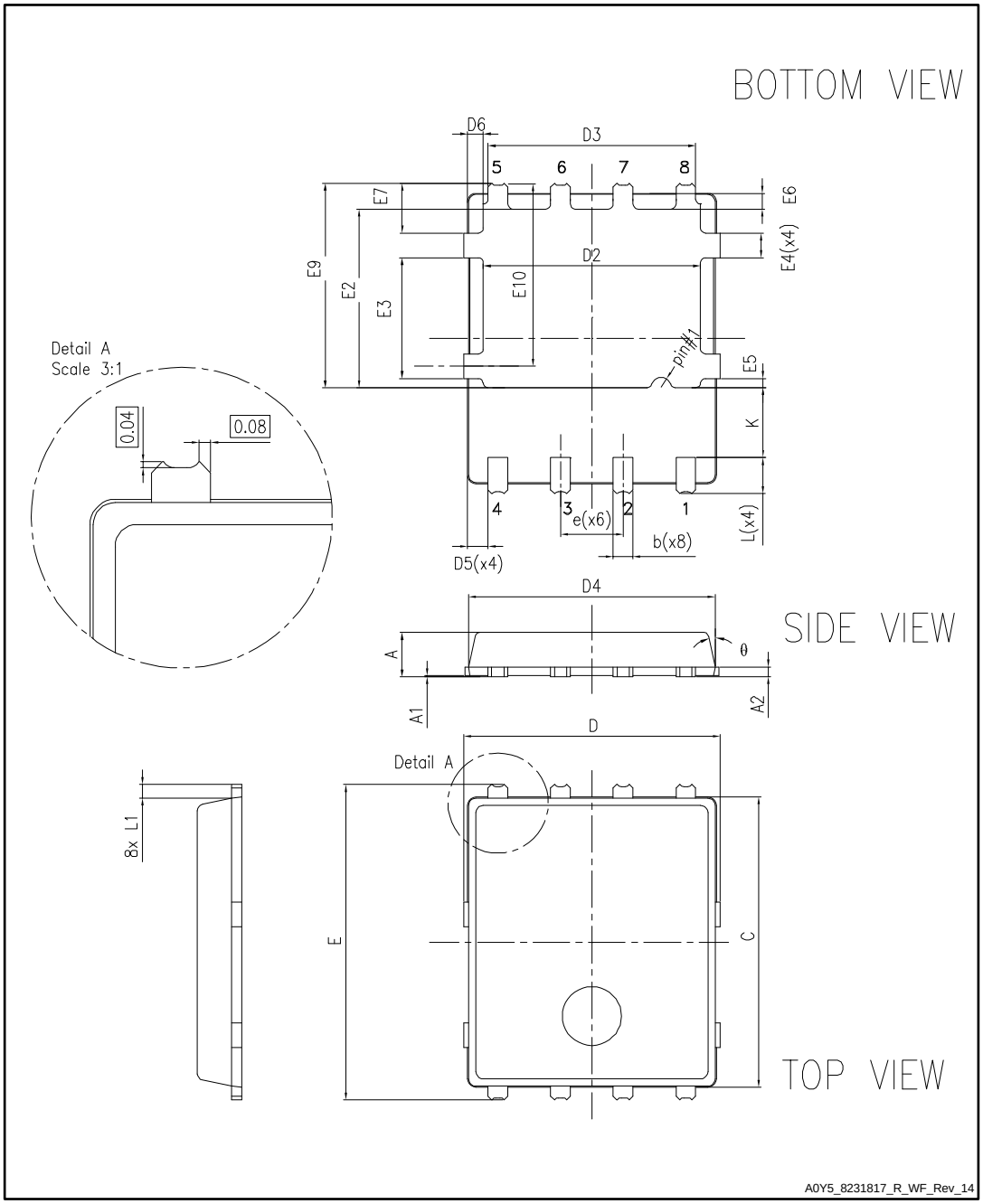
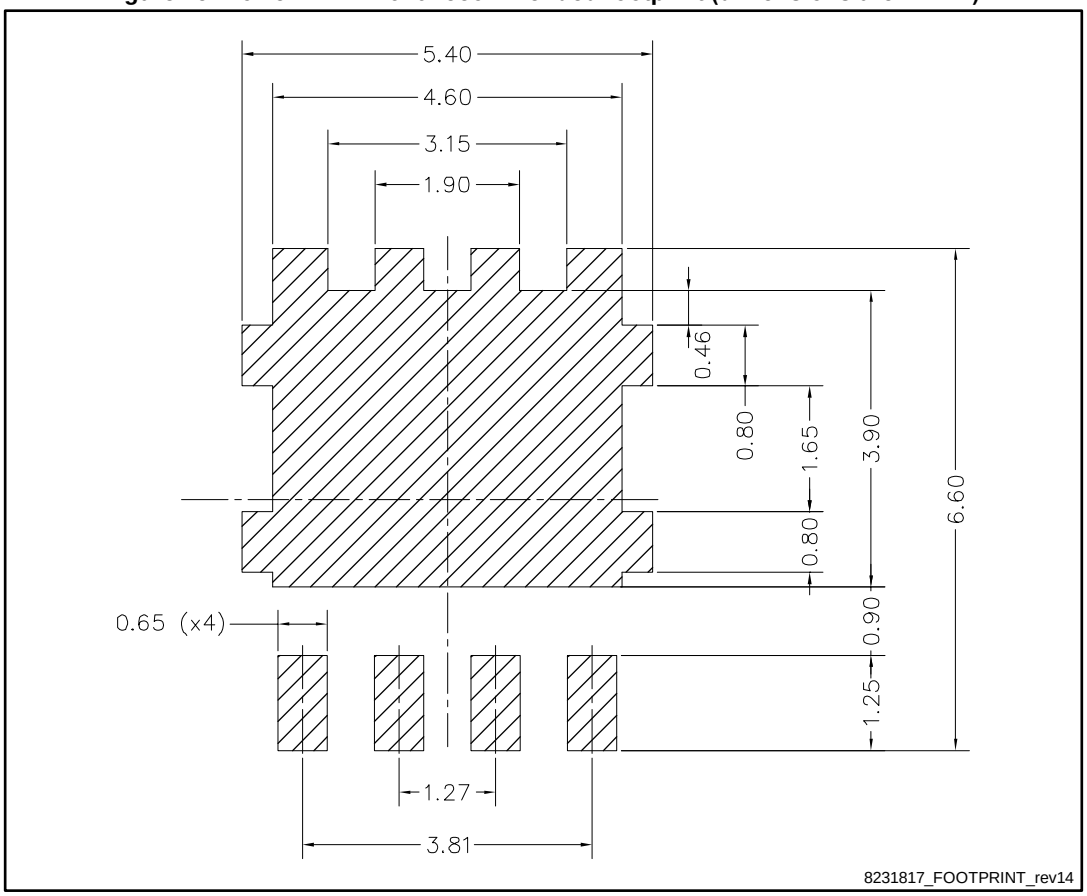


Table 8: PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
Θ	0°		12°

Figure 19: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 20: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

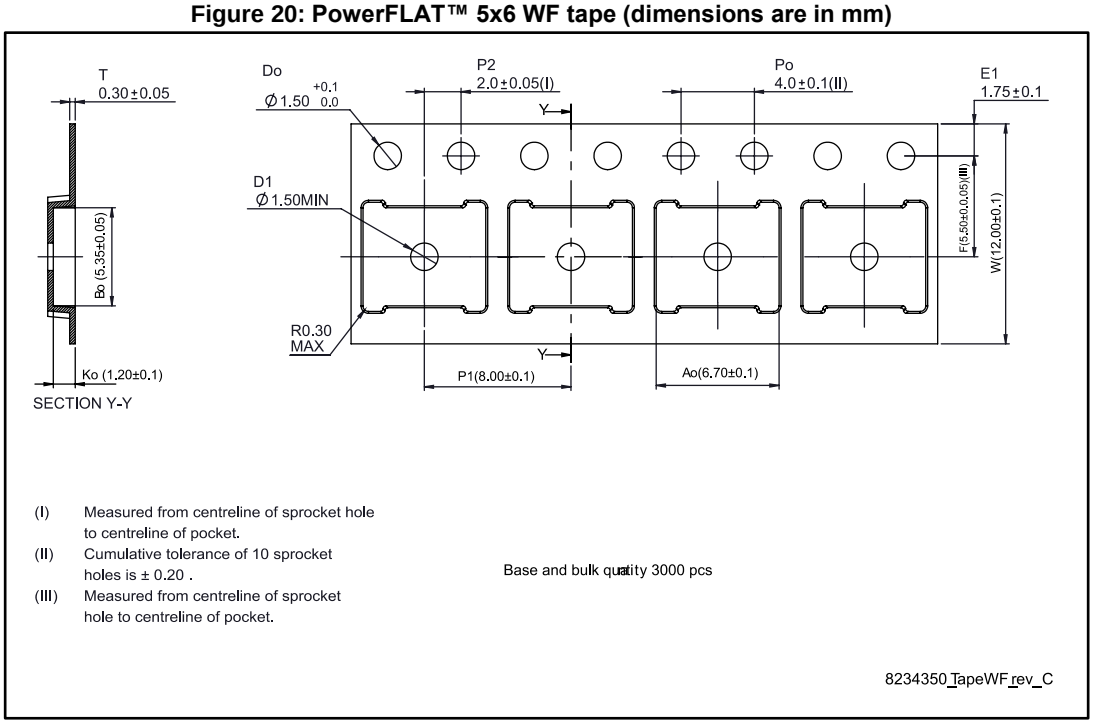


Figure 21: PowerFLAT™ 5x6 package orientation in carrier tape

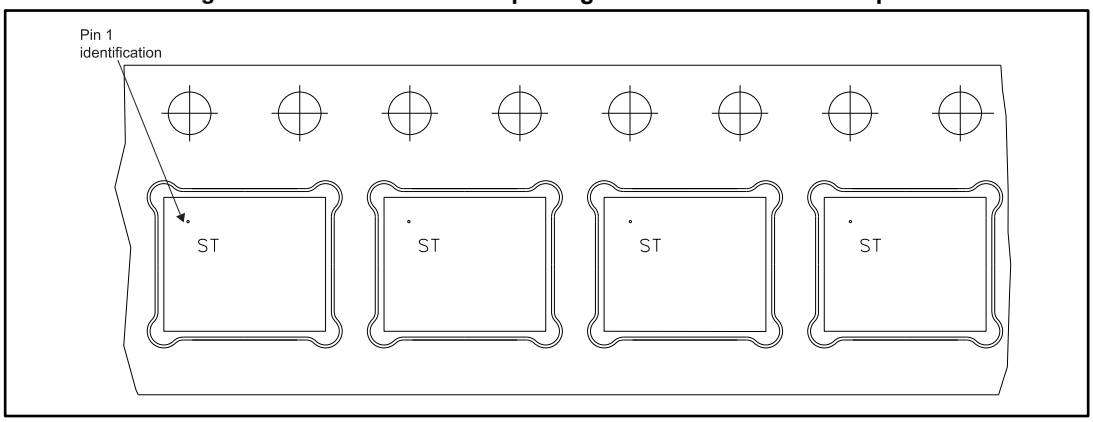
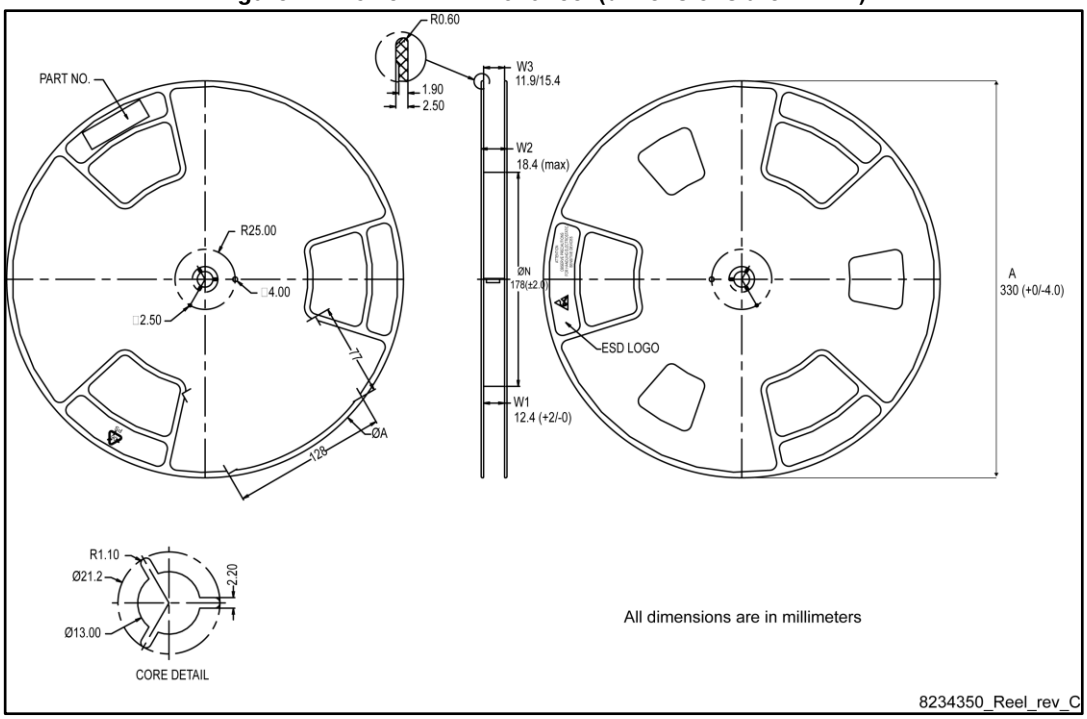


Figure 22: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
14-Oct-2014	1	First release.
10-Feb-2015	2	Updated *Table 4: On/off states, Table 5: Dynamic, Table 6: Switching times, Table 7: Source drain diode* and *Section 4: Package mechanical data.*
26-May-2015	3	Updated title and features. Document status from preliminary to production data.
13-Feb-2017	4	Modified features on cover page. Modified *Table 2: "Absolute maximum ratings"* and *Table 5: "Dynamic"*. Minor text changes.

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